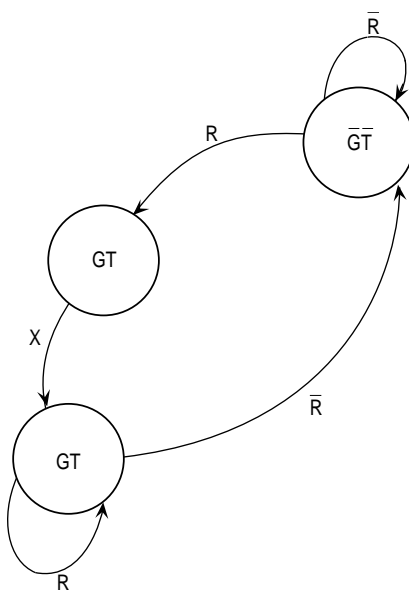


Addendum To
M68000 8-/16-/32-Bit Microprocessor Users Manual

Page	Description
2-5	Table 2-1 Notes. Change "CP = Program Counter" to "PC = Program Counter".
5-17	The 2-wire bus arbitration in Figure 5-18 is incorrect and should be replaced by the following figure.



(b) 2-Wire Bus Arbitration

Figure 5-18. Bus Arbitration Unit State Diagrams

11-1

Replace the table following paragraph 11.1. with the following table.

Case Packages	Suffix	Pins	68000	68008	68010	68HC000	68HC001	68EC000
740-03	L	64	X					
767-02	P	48		X				
754-01	R & P	64	X		X	X		
765A-05	R	68	X		X			
765A-05	RC	68	X		X	X	X	
778-02	FN	52		X				
779-02	FN	68	X		X	X	X	X
847-01	FC	68				X	X	
840B-01	FU	64						X

Note: 1. L = Cermic DIP
P = Plastic DIP
RP = Plastic Pin Grid Array
RC = Pin Grid Array, Gold Lead Finish
FN = Plastic Quad Pack (PLCC)
FC = Plastic Quad (Gull Wing)
FU = Plastic Quad Flat Pack (14 x 14mm)

Note: 2. For ordering information refer to Hi-Performance Embedded Systems Division Fact Sheet SG167/D. This document is published quarterly and may be ordered from the Literature Distribution Center or from your local sales office.

Page	Description
11-4	In Figure 11-3 68-Lead Quad Pack (1 of 2). Pins 13 and 14 are labeled incorrectly. Pin 13 should be labeled $\overline{B}R$ not $\overline{B}GACK$. Pin 14 should be V_{CC} not $\overline{B}R$.
11-5	In Figure 11-3 68-Lead Quad Pack (2 of 2). Pin 31 is labeled incorrectly. Pin 31 should be labeled A0 not NC.
11-7	In Figure 11-6. 64-Lead Quad Flat Pack. Add FU Suffix after 64-Lead Quad Flat Pack.
11-7	Replaced Figure 11-6 with the following figure .
11-10	Figure 11-9. Delete this figure. The LC Package is no longer available.

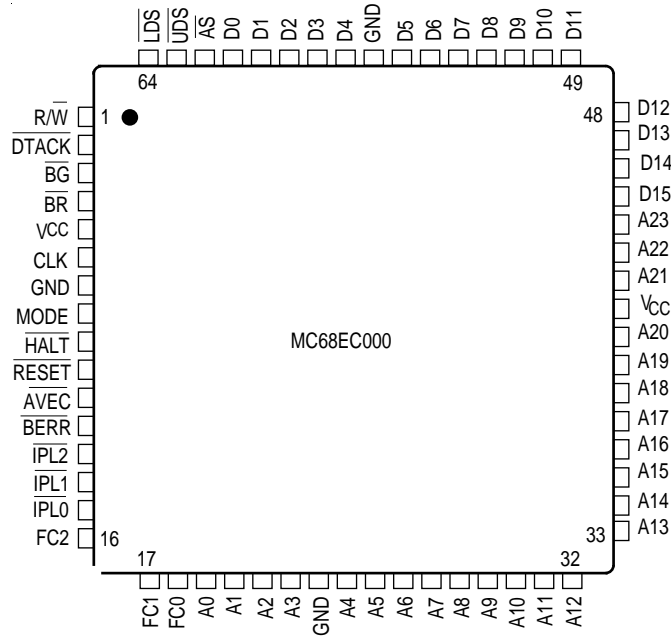


Figure 11-6. 64-Lead Quad Flat Pack—FU Suffix

11-14

In Figure 11-13 Case 779-02—FN Suffix. In Note 1, change 52 Leads to 68 Leads.

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